CLAIMS

1. A monitor system for a semiconductor process comprising:

a test wafer including at least one sensor, the test wafer being positionable on a supporting structure in a process chamber of a semiconductor processing system;

an interface including at least one contact electrically connectable to the sensor when the test wafer is positioned on the supporting structure; and

circuitry electrically connectable to the contact and designed to process signals transmitted from the sensor.

2. The monitor system of claim 1, wherein the test wafer includes a plurality of sensors on a front side of the test wafer.

3. The monitor system of claim 2, wherein the sensors are distributed over a majority of the surface area of the front side of the test wafer.

4. The monitor system of claim 1, wherein the test wafer includes a plurality of contact pads on a back side of the test wafer.

5. The monitor system of claim 4, wherein each contact pad is electrically connected to a corresponding sensor via a wire that extends through the test wafer to define a signal pathway.

6. The monitor system of claim 5, wherein the test wafer comprises an insulating material surrounding each signal pathway.

7. The monitor system of claim 4, wherein the interface includes a plurality of contact pins, each contact pin being in contact with a corresponding contact pad of the test wafer when the test wafer is positioned on the supporting structure.

8. The monitor system of claim 7, wherein the contact pins are spring-loaded.

9. The monitor system of claim 7, wherein each contact pin is connected to an electrical lead that is connected to the circuitry.

10. The monitor system of claim 1, wherein the interface is mountable to the supporting structure.

11. The monitor system of claim 1, wherein the circuitry is external of the process chamber.

12. The monitor system of claim 1, wherein the circuitry is designed to process signals transmitted from the sensor to determine one or more properties related to the semiconductor process.

13. The monitor system of claim 12, wherein one or more of the properties characterizes the efficiency of an ion beam neutralization process.

14. The monitor system of claim 1, wherein the circuitry measures at least one property selected from the group consisting of net floating potential, net current density, electron energy distribution at the front side of the test wafer, and displacement current.

15. The monitor system of claim 1, further comprising a data acquisition system associated with the circuitry.

16. The monitor system of claim 15, wherein the data acquisition system includes a monitor capable of displaying outputs of the circuitry in real-time with the semiconductor process.

17. The monitor system of claim 15, wherein the data acquisition system is connectable to the semiconductor processing system and output signals from the data acquisition system control one or more process parameters.

18. The monitor system of claim 17, wherein output signals from the data acquisition system control one or more process parameters of a plasma flood gun in the semiconductor processing system constructed and arranged to introduce electrons into an ion beam.

19. The monitor system of claim 1, wherein the semiconductor processing system comprises an ion implantation system.

20. The monitor system of claim 1, wherein the signals are transmitted from the sensor to the circuitry in real-time with the semiconductor process.

21. A monitor system for a semiconductor process including a test device positionable within a process chamber of an ion implantation system using a wafer handling system, the test device able to transmit signals to circuitry of the monitor system in real-time with the semiconductor process.

22. The monitor system of claim 21, wherein the test device is free of hard wiring.

23. The monitor system of claim 21, wherein the test device comprises a test wafer.

24. A test wafer comprising:

at least one sensor on a front side of the test wafer;

at least one contact pad on a rear side of the test wafer; and

a conducting wire extending through the test wafer to electrically connect the sensor to the contact pad.

25. The test wafer of claim 24, wherein the test wafer comprises a plurality of sensors and contact pads.

26. The test wafer of claim 25, wherein each sensor is connected to a corresponding contact pad with a single conducting wire to define a signal pathway.

27. The test wafer of claim 26, further comprising insulating material surrounding the signal pathways.

28. The test wafer of claim 24, wherein the sensors are distributed over a majority of the surface area of the front side of the test wafer.

29. The test wafer of claim 24, wherein the contact pads are distributed around a periphery of the test wafer.

30. The test wafer of claim 24, further comprising a conducting layer connectable to ground.

31. An interface device capable of establishing electrical contact with a test wafer positioned on a supporting structure, the interface device including a plurality of contact pins, each contact pin being in contact with a corresponding contact pad of the test wafer when the test wafer is positioned on the supporting structure.

32. The interface device of claim 31, further comprising a ring assembly, wherein the contact pins are positioned along a diameter of the ring assembly.

33. The interface device of claim 31, wherein the contact pins are spring-loaded.

34. The interface device of claim 33, further comprising an adjuster constructed and arranged to adjust the spring loading of the contact pins.

35. The interface device of claim 31, further comprising an electrical lead connected to each contact pin.

36. The interface device of claim 31, further comprising a mounting element constructed and arranged to mount the interface device to a supporting structure.

37. A method of monitoring a semiconductor process comprising:

exposing a test wafer including at least one sensor to a semiconductor process;

transmitting signals from the sensor on the test wafer to circuitry; and

processing the signals using the circuitry.

38. The method of claim 37, further comprising positioning the test wafer in a process chamber using a wafer handling system prior to exposing the test wafer to the semiconductor process.

39. The method of claim 37, comprising processing the signals using the circuitry in real-time with the semiconductor process.

40. The method of claim 37, comprising processing the signals to determine one or more properties related to the semiconductor process.

41. The method of claim 40, comprising processing the signals to determine one or more properties that characterize the efficiency of an ion beam neutralization process.

42. The method of claim 40, comprising processing the signals to determine at least one property selected from the group consisting of net floating potential, net current density, electron energy distribution at the front side of the test wafer, and displacement current.

43. The method of claim 40, further comprising adjusting at least one semiconductor process parameters in response to property data.

44. The method of claim 43, comprising adjusting an ion beam charge neutralization process in response to property data.

45. The method of claim 43, wherein an output signal from a data acquisition system adjusts the semiconductor process parameter.

46. The method of claim 40, further comprising displaying property data in real-time with the semiconductor process.

47. The method of claim 37, comprising exposing a test wafer to an ion implantation.

48. The method of claim 47, further comprising generating an ion beam having a net positive charge and introducing electrons into the ion beam to neutralize the ion beam charge prior to the ion beam impinging upon the test wafer.